ChipsC² LT
CHIPS COMPETENCE CENTER

DATABASE OF RESOURCES

Project number: 101217991

Lithuanian Chips Competence Centre

Deliverable No. D2.1

Version 1.3

CENTER FOR PHYSICAL SCIENCES AND TECHNOLOGY

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1 EXECUTIVE SUMMARY

This deliverable presents the Database of Resources for ChipsC²-LT, providing a comprehensive inventory of semiconductor equipment, design tools, and technical expertise available through the Lithuanian Chips Competence Centre. The database serves as the foundation for establishing ChipsC²-LT as a one-stop shop facility for the local industry, particularly SMEs and startups working with advanced semiconductor technologies. The ChipsC²-LT consortium brings together four leading Lithuanian research and academic institutions: FTMC as coordinator, VU, VGTU, and KTU. This initial version of the database focuses on technological processing equipment, design tools and testing equipment, with characterisation capabilities to be incorporated in subsequent updates.

Design and simulation resources at VGTU and KTU include industrial-grade EDA tools: Cadence for analogue and mixed-signal IC design, supporting nodes from 180 nm to 3 nm; Siemens for physical verification and sign-off; Keysight PathWave for RF and microwave design up to 110 GHz; and Altium for PCB development. Process Design Kits from major foundries enable tape-out-ready designs.

Epitaxial growth systems at FTMC provide MBE capabilities for III-V compound semiconductors, including arsenides, antimonides, and bismides. At the same time, VU operates MOCVD for III-nitride materials (GaN, AlN, InGaN, AlGaN), supporting the development of LED, HEMT, and photonic devices.

Front-end processing capabilities include electron beam lithography at KTU with nanometre-scale positioning accuracy, laser lithography at VU and FTMC with features down to 0.6 µm, and photolithography at FTMC for wafers up to 150 mm. Thin-film deposition is supported by magnetron sputtering, electron-beam evaporation, ion beam deposition, ALD, and PECVD systems. Dry etching capabilities include ICP-RIE for III-V semiconductors and silicon-based materials. Rapid thermal annealing systems operate up to 1200°C, with heating rates to 150 K/s.

Packaging and assembly resources cover die bonding with placement accuracy of 0.5 µm, thermosonic wire bonding for gold, aluminium, and ribbon interconnects, and a complete PCB assembly line including solder paste printing, pick-and-place, and reflow soldering.

Testing capabilities include precision probe stations with semiconductor parameter analysers at all partner institutions, providing DC measurements from 1 pA to 1 A, pulsed I-V characterisation, C-V measurements from 1 kHz to 10 MHz, and RF S-parameter measurements up to 26.5 GHz. Temperature-controlled measurements are available from -60°C to +350°C.

All equipment is housed in cleanroom facilities classified ISO 5 to ISO 8, ensuring appropriate contamination control for semiconductor processing.

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2 INTRODUCTION

2.1 Purpose and Scope

This document presents a comprehensive catalogue of equipment and resources allocated by consortium partners for ChipsC²-LT activities. As specified in Grant Agreement No. 101217991, the inventory covers all equipment for semiconductor processing, assembly, packaging, testing, and characterisation available at partner institutions, together with design and simulation tools and knowledge in the field of ChipsC²-LT specialisation.

The database covers resources from four institutions, and each equipment entry provides technical specifications, operational parameters, material compatibility, cleanroom classification (where applicable), and contact information for the responsible person.

2.2 ChipsC²-LT Focus Areas

The resources documented in this database support ChipsC²-LT services in four specialisation areas that reflect partner competencies and local industry needs:

- **Chip Design:** Analog, digital, RF, and mixed-signal IC design with access to industrial EDA tools and foundry PDKs.
- **Power Electronics:** Wide bandgap semiconductor technologies, particularly GaN and SiC device development.
- **Heterogeneous Integration:** Advanced packaging techniques including die bonding, wire bonding, and multi-material integration.
- **Photonic Integrated Circuits:** III-V compound semiconductor epitaxy, optoelectronic device fabrication, and THz.

2.3 Document Structure and Updates

The resource catalogue is organised by technology category, following the semiconductor value chain from design and materials through front-end processing, back-end assembly, and testing. This structure enables users to identify relevant capabilities for specific project requirements.

This database is maintained as a living document. Updates will be incorporated through subsequent WP2 deliverables as infrastructure upgrades are implemented and the service portfolio evolves throughout the project period.

2.4 Database Structure and Maintenance

The resource information presented in this document is maintained in a structured format to enable efficient updates and queries. The underlying data is organised in interconnected tables covering the following entities:

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Equipment Registry: core technical data for each system, including equipment identifier, name, manufacturer, year of acquisition, partner institution, technology category, key specifications, operational parameters, material restrictions, cleanroom classification, and responsible contact person.

Partner Facilities: cleanroom and laboratory infrastructure at each institution, including facility type, classification (ISO class), location, and available capabilities.

Contact Directory: responsible persons for each equipment category, with their department affiliations and contact details.

Each equipment entry in this document corresponds to a record in the registry, ensuring consistency between the published catalogue and operational data. The database structure supports:

- Filtering by partner, technology category, or capability
- Identifying responsible contacts for access inquiries
- Planning infrastructure upgrades (linking to D2.2)
- Developing service portfolio (linking to D2.4 - D2.6)

Updates to the registry follow the resource management procedures established in D2.7. Partner institutions are responsible for maintaining accurate information for their equipment, with FTMC coordinating consolidated updates aligned with project reporting periods. The current version of this database covers technological processing equipment, design tools and testing equipment. Characterisation and advanced testing equipment will be incorporated in subsequent updates. To facilitate access for potential users, the resource database will be made available through the ChipsC²-LT website in a searchable format, enabling companies to filter equipment by partner institution, technology category, or material compatibility.

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3 RESOURCE CATALOGUE

Electronic Design Automation Software

VGTU and KTU provide a comprehensive design and research environment for CMOS and GaN integrated circuits and advanced electronic systems. Comprehensive services cover the entire microelectronics development cycle, from system-level modelling and schematic creation to layout, verification, and fabrication-ready data generation.
The team operates with industrial-grade EDA tools and process design kits (PDKs), offering:

- Analog, mixed-signal, RF, and microwave circuit design;
- Digital and embedded-system development;
- Multilayer PCB architecture design and validation;
- Transistor-level modelling and electromagnetic analysis;
- Design-rule and layout-versus-schematic (DRC/LVS) verification;
- Generation of GDSII and manufacturing-ready deliverables compliant with foundry specifications.

Each project includes specification and datasheet preparation, project cost and NRE estimation, and risk-controlled planning to ensure successful transition from concept to fabrication.

Software	Altium Designer Academic License (Altium Ltd., 2025)	VGTU, KTU
	Electronic Design Automation (EDA) Software for PCB Design. • Design domains: schematic capture, PCB layout, 3D modelling, and simulation; • Supported layers: up to 32 signal layers and 16 plane layers; • Integrated MCAD collaboration (STEP/3D export, mechanical clearance); • Real-time design rule checking (DRC) and electrical validation; • Signal integrity and power integrity analysis tools included; • Integration with version control (SVN, Git) and cloud workspace (Altium 365); • Output formats: Gerber, ODB++, IPC-2581, BOM, Pick & Place data. **Contact persons:** Dr. Vaidotas Barzdėnas Faculty of Electronics VILNIUS TECH	

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	vaidotas.barzdenas@vilniustech.lt Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Software	**Keysight EEsof EDA / PathWave Design Academic License (Keysight Technologies, 2025)**	**VGTU, KTU**
	Electronic Design Automation (EDA) Software for RF, Microwave, and High-Speed Design • Design domains: RF, microwave, analog/mixed-signal, and high-speed digital; • Frequency range: DC to 110 GHz (depending on license and model); • Simulation types: linear, harmonic balance, transient, envelope, EM (Momentum/FEM); • Integrated layout, DRC/LVS, and EM co-simulation (3D EMPro interface); • System-level design and verification using PathWave SystemVue; • Schematic-driven PCB and MMIC design with foundry PDK integration; • Supported PDKs: GaN, GaAs, CMOS, SiGe (IHP, WIN, TSMC, UMS, etc.). **Contact persons:** Dr. Vaidotas Barzdėnas Faculty of Electronics VILNIUS TECH vaidotas.barzdenas@vilniustech.lt Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Software	**Cadence IC Package Academic License (Cadence Design Systems, 2025)**	**VGTU, KTU**
	Integrated Circuit Design Software Suite • Design domains: Analog, Digital, RF, and Mixed-Signal ICs; • Supported technologies: 180 nm – 3 nm CMOS/BiCMOS nodes;	

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	• Simulation engines: Spectre, APS, QRC, and ADE-XL integrated flow; • Layout and physical verification: Virtuoso Layout Suite, Assura, and PVS; • Packaging design: Allegro Package Designer with SiP co-design capability; • Schematic-driven layout, parametric cells, and design reuse automation; • Process Design Kit (PDK) integration for TSMC, GF, IHP, and UMC technologies. **Contact persons:** Dr. Vaidotas Barzdėnas Faculty of Electronics VILNIUS TECH vaidotas.barzdenas@vilniustech.lt Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Software	**IC Nanometer Design Software Suite Academic License (Siemens EDA, 2026)**	**VGTU, KTU**
	Software Package for Integrated Circuit Design • Custom IC design and layout – IC Station, Aprisa, Calibre Design Enhancer for schematic entry, floor-planning, and physical design; • Analog, mixed-signal, and digital simulation – Analog FastSPICE Platform, Eldo, Questa ADMS, and ModelSim / Questa Sim; • Physical verification and sign-off – Calibre DRC, LVS, xACT, and Calibre PERC for design rule checking, layout-vs-schematic comparison, and parasitic extraction; • Timing, power, and reliability analysis – PowerPro, Timing Designer, Calibre Reliability tools for performance optimisation and low-power design; • Design-for-manufacturability (DFM) and yield enhancement – Calibre DFM and YieldAnalyzer modules; • Library and cell-based design – Library Characterisation Suite for creating and validating standard-cell and I/O libraries; • Integration with foundry process design kits (PDKs) and support for nanometer-scale CMOS and FinFET technologies.	

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Epitaxial Growth

Epitaxial growth is a fundamental technique in semiconductor fabrication, enabling the deposition of highly ordered crystalline layers on a substrate with matching orientation. This process allows for tailoring layer thickness, composition, and defect density, which directly influences the performance of microchips, power electronics, and optoelectronic components. Several approaches exist, including liquid-phase epitaxy, vapour-phase epitaxy, and molecular beam epitaxy (MBE), each offering distinct advantages in precision, purity, and scalability. Among them, MBE stands out for research and development applications because it allows atomic-level control of film growth under ultra-high vacuum conditions, making it ideal for producing complex heterostructures and quantum-scale architectures that drive innovation in next-generation semiconductor devices.

Molecular Beam Epitaxy	Compact MBE System SVT-V-2 (SVT Associates, 2009)	FTMC
	The system is used for materials research, namely, III-V compound semiconductors. • 7 sources; • Group III: In, Ga and Al; • Group V: As and Bi; • Valved cracker for As_2; • Dopants: for n-type – Si, for p-type – Be; • Sample temperature up to 1000 °C; • Thickness uniformity error <2 % over 2'' Wafer; • Fast action shutters; • Master wafer shutter; • Configuration: Load lock and growth chamber; • Growth module is equipped with the integrated ion and Titanium sublimation pump system (base vacuum level $5 \cdot 10^{-5}$ Torr); • The load lock is equipped with the turbo molecular (base vacuum level $5 \cdot 10^{-8}$ Torr); • RoboMBE process automation for growth recipe operation; • Materials allowed: substrates GaAs, InP; • Restrictions: Substrates 2" or ¼ 2". **Cleanroom class:** ISO7 **Contact person:** Dr. Vaidas Pačebutas Department of Optoelectronics Center for Physical Sciences and Technology vaidas.pacebutas@ftmc.lt	
Molecular Beam Epitaxy	**MBE System Veeco GENxplor R&D (Veeco, 2015)**	**FTMC**

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	GENxplo MBE system is designed for the epitaxial growth of high-quality III-V semiconductor compounds with very high deposition control accuracy on substrates up to 3'' in diameter for R&D and small-scale manufacturing purposes. • Extremely high composition and thickness accuracy (error <1.5 %); • 10 Sources; • Group III: In, 2xGa and Al; • Group V: As, Sb and Bi; • Cracker for Sb and As_2; • Dopants: for n-type – Si, Te, for p-type – Be; • Fast action shutters; • Master wafer shutter; • Configuration: Load lock and growth chamber; • Growth module is equipped with the integrated ion and Titanium sublimation pump system (base vacuum level $5 \cdot 10^{-9}$ Torr); • The load lock is equipped with the turbo molecular (base vacuum level $5 \cdot 10^{-8}$ Torr); • Materials allowed: Substrates GaAs, InP, InAs, GaSb, Si; • Restrictions: Substrates 2", ¼ 2", 3" or ¼ 3". Sample temperature up to 1850 °C; **Cleanroom class:** ISO7 **Contact person:** Dr. Vaidas Pačebutas Department of Optoelectronics Center for Physical Sciences and Technology vaidas.pacebutas@ftmc.lt

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Lithography

Lithography is a microfabrication process used to create precise patterns on a substrate. It works by applying a radiation-sensitive material (resist) to the surface, exposing it to light, electrons, or other radiation through a mask or direct writing, and then developing the resist to reveal the desired pattern. After patterning, lithography is often combined with etching (to remove material in unprotected areas) or lift-off (to deposit thin films only in selected regions). This enables the fabrication of features like trenches, vias, and metal layers.

Available lithography techniques across partner institutions are electron beam lithography, laser lithography and photolithography. All lithography systems are equipped with resist pre- and post-processing tools for spin coating, baking, and developing.

Electron beam lithography	e-LiNE plus (RAITH GmbH, 2013)	KTU
	System for nanolithography, nano structuring and materials surface and composition analysis: • Electron beam energy is changing in the range 20 V – 30 kV; • Beam current 5 pA – 1.5 nA; • 1 nm positioning accuracy in a 100 × 100 mm field; • Diameter of round sample: up to 100 mm (4“), size of rectangular sample: up to 102 × 102 mm; • Magnification of scanning electron microscope with “in-lens” and Everhart-Thornley type detectors up to x1,000,000; • Energy resolution of energy dispersive spectrometer Bruker QUANTAX 200 with 5th generation Si detector: < 129 eV, allows to detect elements from Be (Z = 4) to Am (95); • Writing speed: 0.125 Hz – 20 MHz pixel frequency; • Beam size: >1.6 nm at 20 keV; • Stitching accuracy: >40 nm (mean+3σ). **Cleanroom class:** ISO5 **Contact person:** Dr. Mindaugas Juodėnas Institute of Materials Science Kaunas University of Technology mindaugas.juodenas@ktu.lt	

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Laser lithography	Microtech LaserWriter LW405D (Microtech s.r.l., 2020)	VU
	Laser writing tool for photolithographic mask fabrication and for direct in situ processing on semiconductor substrates: • Direct laser writing sources: - 405 nm GaN laser, 60 – 100 mW (general lithography, AZ-series and thin SU-8 <10 µm); - 375 nm GaN laser, 60 mW (thick SU-8 <50 µm, UV-sensitive resists); • Write modes: beam-scan, stage-scan, vector, contour, flash; • Optical resolutions (interchangeable focusing lenses): - 0.6 µm (feature positioning 0.1 µm); - 1.6 µm (feature positioning 0.2 µm); - 4 µm (feature positioning 0.4 µm); - 8 µm (feature positioning 0.8 µm); - 5 µm (feature positioning 0.5 µm, high depth-of-focus ≈ 40 µm, 375 nm laser); • Write area: 100 × 100 mm² (substrates ≤6″ × 6″ or 150 × 150 mm); • Substrate/sample thickness: 0 – 4 mm (standard), up to 10 mm without holder plate; • Stage resolution: 10 nm (dual-beam XY laser interferometer optional); • Focusing: optical autofocus with 4 mm range and tilt compensation (≤2°); supports non-planar substrates (curvature radius ≥75 mm); • Minimum linewidth: 0.6 µm at 405 nm (High-NA lens); • Overlay accuracy: sub-micron (<0.5 µm typical with interferometer); • Exposure dose: step or continuous control (1 – 200 mJ/cm²); • Stage velocity: 0 – 10 mm/s (all modes); beam-scan speeds 2 – 450 mm²/min depending on resolution; • Grey-level patterning for 3D relief and diffractive optics; • Video-metrology mode: 100 – 800 µm fields of view, 0.2 µm optical resolution; • Software: PhotonSteer® v12 (CleWin-5 layout integration, GDSII/DXF/CIF formats, automatic recipe database and alignment tools). **Cleanroom class:** ISO8 **Contact person:** Dr. Roland Tomašiūnas Institute of Photonics and Nanotechnology	

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	Vilnius University roland.tomasiunas@ff.vu.lt	
Laser lithography	**DWL66+ Laser Lithography System (Heidelberg Instruments GmbH, 2015)**	**FTMC**
	Laser writing system for maskless exposure on metalised plates or semiconductor wafers: • 405 nm single-mode diode laser light source; • Laser power 350 mW; • Write heads: - 10 mm focal plane: critical dimension ~2 µm, write speed 140 mm^2/min; - 2 mm focal plane: critical dimension ~800 nm, write speed 6 mm^2/min; • Minimal wafer size 1 × 1 cm^2; • Maximum wafer size 20 × 20 cm^2; • Working area 200 × 200 mm; • Standard writing and vector exposure modes (vectorial mode resolution >2 µm, stitching-free lines); • Interferometric stage position measurement; • Stage resolution 10 nm; • Automatic focus: pneumatic, optical; • Minimal size of wafer 1 × 1 cm^2; • Double side alignment (only for 10 × 10 cm^2 sized wafers); • Design data file in DXF, Gerber, GDSII, or CIF format. **Cleanroom class:** ISO5 **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	
Photolithography	**MA/BA6 Gen4 Mask aligner (SUSS MicroTec Lithography GmbH, 2019)**	**FTMC**
	Photolithographic system for automated 1:1 direct projection of structures from a photo mask to photo-sensitive coated substrates: • UV-LED Light Source provides a spectrum of several wavelengths: - 365 nm (i-line); - 405 nm (h-line); - 436 nm (g-line); • Automatic wedge compensation system in contact or without contact between mask and wafer (with reference balls);	

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	• Alignment gap programmable from 1 – 1000 µm; • Resolution 1 µm; • Stage movement range: X ±5.0 mm, Y ±5.0 mm, Theta ±5°; • Reset movement to ZERO position after each exposure; • Protection of the mask and wafer when in contact by locking the motors to prevent stage movement; • TSA/BSA face-to-face microscope stage with motorized X-Y-manipulator; • Manual loading and unloading of wafer, single substrates or substrate stack; • Wafer size up to 150 mm diameter; • Mask holders: - for masks from 5“ × 5“ to 6“ × 6“, exposure opening for wafers ø100 mm; - for masks from 3.5“ × 3.5“ to 5“ × 5, exposure opening for wafers ø2” – 3”; - for mask 4” × 4”, exposure opening for wafers 20 × 20 mm; • Chucks for wafer 1”, 2", 3“, 100 mm diameter. **Cleanroom class:** ISO5 **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt

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Physical Vapour Deposition

PVD is a vacuum-based technique for depositing thin films by vaporising material from a solid source using thermal, electron-beam, or plasma-assisted mechanisms and condensing it onto the substrate. Standard methods include thermal evaporation and e-beam evaporation for high-purity metal films with well-controlled deposition rates, as well as DC and RF magnetron sputtering, which enable dense, adherent coatings of metals, dielectrics and oxides. Advanced systems offer loadlock sample handling, multi-target sputtering, reactive deposition, and high-purity films for applications in microelectronics, optics, and protective coatings.

Electron-Beam Evaporation	CreaPhys / MBraun UNIvap 5 S (CreaPhys GmbH, part of MBraun Group, 2021)	VU
	• Process method: Electron-beam evaporation (metals, semiconductors, dielectrics); • Base pressure: <$5 \cdot 10^{-7}$ mbar (dry pump-down ≤2 h); • Working pressure: 10^{-6} – 10^{-5} mbar typical; • Vacuum system: Edwards XDS35i scroll pump (28 m³/h) + Pfeiffer HiPace 800 turbo pump (685 L/s); • Vacuum chamber: Rectangular 304 SS 500 × 545 × 600 mm (internal); • Control: Siemens S7-1500 PLC with 7″ touch HMI (automatic pump/vent/heater/shutter sequencing); • E-beam source: EB M-7 II with WARP 6 II beam deflection, STINGRAY DC supply (2 – 10 kV, 0 – 600 mA, 6 kW max); • Crucible pockets: 6 × 6 cm³ with motorized optical position feedback; • Sweep modes: sine/triangle / square/custom, ±3 A at 24 VAC, 0 – 100 Hz; • Substrate rotation: 0 – 30 rpm (continuous, vacuum feedthrough); • Substrate heater: ceramic IR type, RT – 500 °C (2 × 400 W, Type K thermocouple feedback); • Substrate size: up to 100 × 100 mm or Ø 150 mm (1 × 150 mm wafer or 4 × 25 × 25 mm samples); • Thickness/rate control: 6 MHz water-cooled QCM + MB/SQC-310 controller (±0.03 Hz at 0.1 s ≈ 0.01 Å·s^{-1} resolution); • Uniformity: < ±5 % across 100 mm substrate (at 30 rpm); • Qualified and approved evaporation materials: Ti, Ni, Al, Au, Others: Metals and semiconductors compatible with E-	

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	beam source under 10^{-6} mbar conditions may be qualified after approval; • Restrictions (size, materials prohibited, etc.): - Substrate size: Ø ≤150 mm or 100 × 100 mm; - Restricted materials causing outgassing or corrosive vapours (fluorides, hydrides, oxides with high oxygen release); - Atmosphere: vacuum or dry nitrogen vent only. **Cleanroom class:** ISO8 **Contact person:** Dr. Roland Tomašiūnas Institute of Photonics and Nanotechnology Vilnius University roland.tomasiunas@ff.vu.lt

Magnetron sputtering	**EvoVac (Angstrom Engineering Inc, 2015)**	**FTMC**
	• Process: Thin layer deposition; • Materials for deposition: Au, Cr, Ni, Ti, Mo, Al, Cu, In, Sn, Ag and their oxides; • Chamber temperature: 20 – 600 °C; • Working pressure: 2 – 25 mTorr; • Maximum substrate size: up to 4”; • Substrates: Semiconductors, metals, glasses (materials with low vapour pressure/ compatible with vacuum chamber); • Deposited layer thickness – 2 – 500 nm (it is possible to deposit thicker layers, but it is not practical); • Process gases: O_2, Ar; • Equipment is fitted with four magnetrons: - RF up to 300 W; - DC up to 1.2 kW DC Glassman Sputter; - RF or DC; - HiPIMS (High Power Impulse Magnetron Sputtering) Advanced Energy 5 kW Pinnacle Plus DC; • Additional information: - Ion beam - Kaufman and Robinson EH400 5 A (For cleaning the sample or removing the layer); - Possibility to change distance between sample and magnetron (up to 20 cm); - Rotating sample holder for even coating (up to 50 rpm);	

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	- Fast loading system (load-lock). **Cleanroom class:** ISO7 **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	
Electron-Beam Evaporation	**VST Model TFDS–870 (Vacuum Systems Technologies and Services Ltd. made in cooperation with MBraun USA, 2012)**	**FTMC**
	• Maximum sample size: up to 3”. If individual samples are smaller, it is possible to fit up to 10 samples as long as the total area remains within a 3-inch diameter limit; • The sample holder can be rotated (0-28 rpm), which would ensure the uniformity of the coated layer on the sample; • Thin-film thickness and deposition rate are controlled with Telemark (Model 880) controller; • Sensor crystal frequency is 6 MHz, resolution (5 MHz – 6 MHz), the measurement speed is 10 measurements/second, and the accuracy of thickness per single measurement. Most frequently used deposition rate 5 A/s; • Materials allowed: - This machine is used to grow contacts on the wafers of various materials such as Au, AuGe12%, Ge, Ti, Ni, Sn, Pt and Al; • Restrictions (size, materials prohibited, etc.): - Using samples with zinc (Zn) is strictly forbidden. **Cleanroom class:** ISO7 **Contact person:** Dr. Andrius Bičiūnas Department of Optoelectronics Center for Physical Sciences and Technology andrius.biciunas@ftmc.lt	
Ion-Beam sputtering	**IBS@LAB (Cutting Edge Coatings GmbH)**	**FTMC**
	• Single-layer and multilayer coatings; • Metals and metal–oxide coatings such as SiO_2, HfO_2, Ta_2O_5, etc; • Physical thickness of coatings from a few nm to tens of μm; • Optical monitoring control. **Cleanroom class:** ISO6	

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	Contact person: Dr. Lina Grinevičiūtė Department of Laser Technologies Center for Physical Sciences and Technology lina.grineviciute@ftmc.lt	
Electron-Beam Evaporation	**VERA 1100 (VTD Vakuumtechnik Dresden GmbH)**	**FTMC**
	• Single-layer and multilayer coatings; • Metals, metal–oxide and fluoride coatings such as SiO_2, HfO_2, MgF_2, etc; • Physical thickness of coatings from a few nm to tens of μm; • Crystal quartz monitoring control. **Cleanroom class:** ISO6 **Contact person:** Dr. Lina Grinevičiūtė Department of Laser Technologies Center for Physical Sciences and Technology lina.grineviciute@ftmc.lt	
Magnetron sputtering	**PVD 225 (Kurt J. Lesker Company Ltd.)**	**FTMC**
	• Single-layer and multilayer coatings; • Metals and dielectric coatings such as Cr, Ag, ITO, etc.; • Physical thickness of coatings from a few nm to tens of μm; • Optical monitoring control. **Cleanroom class:** ISO6 **Contact person:** Dr. Lina Grinevičiūtė Department of Laser Technologies Center for Physical Sciences and Technology lina.grineviciute@ftmc.lt	
Thermal evaporation	**Vacuum evaporation equipment CUBIVAPT**	**KTU**
	• Process method: thermal resistive evaporation for Ag deposition; • Maximum sample size: up to 12”; • Two 15 kW power electron guns; • Two 4 kW power resistive evaporators; • Substrate temperature: 20 – 400 °C; • Vacuum in a chamber: 10^{-3} Pa;	

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	• Film Thickness Control: Quartz crystal microbalance monitor; • Deposition Rate: Adjustable, dependent on material and process parameters; • Rotating substrate holder to ensure even film distribution; • Supports metals with a melting temperature less than tungsten. **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Thermal evaporation	**Vacuum evaporation equipment A7000E**	**KTU**
	• Materials for deposition: Cu, Cr, Au, TiO_2; • Maximum sample size: up to 80 x 80 mm; • A microprocessor and a quartz thickness meter control the thickness of formed samples; • Vacuum in a chamber 10^{-4} – 10^{-5} Pa; • Two 6 kW power electron guns with four rotating position crucibles; • Substrate temperature: 20 – 400 °C. **Cleanroom class:** ISO5 **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Ion-Beam deposition	**Ion-beam diamond-like carbon (DLC) deposition device URM 3.279.053**	**KTU**
	The device is designed for the ion-beam deposition process of DLC from hydrocarbon and dopant materials. • Maximum sample size: up to 80 x 80 mm; • Base pressure in chamber: $4 \cdot 10^{-4}$ Pa; • Pressure during DLC synthesis: $(1\text{-}2) \cdot 10^{-2}$ Pa; • Accelerating potential of ion-beam source: max 2 kV; • Ion beam current density: 0.05 – 0.25 mA/cm^2; • Current of solenoid: 6 A; • Gases: both inert and reactive gases can be used; • Substrates such as Si or most other solids can be used.	

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Chemical Vapour Deposition

Chemical Vapour Deposition enables the formation of high-quality thin films and coatings by introducing reactive precursor gases into a heated chamber, where they decompose or react at the substrate surface. The technique supports a wide range of materials, including semiconductors, oxides, and nitrides, with excellent uniformity across large areas. Variants include Metal-Organic CVD (MOCVD), which uses metal-organic precursors for compound semiconductors such as GaN or InP, and Plasma-Enhanced CVD (PECVD), which introduces plasma to activate reactions at lower temperatures, making it ideal for temperature-sensitive substrates. Typical applications include device passivation, optical coatings, epitaxial growth for optoelectronics, and advanced nanostructure fabrication.

Metal-Organic Chemical Vapour Deposition	AIXTRON 3×2FT (AIXTRON Ltd., 2009)	VU
	• Growth temperature range: 450 – 1200 °C (Eurotherm 2704 + IMPAC IGA 50 control); • Reactor pressure range: 150 – 800 mbar (MKS 651 PID + Baratron feedback); • Showerhead–susceptor gap: 5 – 25 mm (standard ≈ 11 mm); • Susceptor rotation: 50 – 150 rpm, max 300 rpm (ferrofluidic feedthrough); • Independent gas flow control for TMGa, TMAl, TMIn, TEGa, Cp2Mg, NH_3, SiH4, H_2/N_2; • Substrate temperature uniformity ±5 °C across 2″ wafers; • In-situ optical reflectometry for real-time growth-rate & thickness monitoring; • Three-zone tungsten-coil heater (center/middle/edge zones A–C) for uniformity correction; • Materials allowed: - GaN (low-T 550 – 650 °C / high-T 1000 – 1100 °C); - AlN (few nm to hundreds nm, buffer or nucleation layers); - InN (450 – 550 °C range); - $In_xGa_{1-x}N$ (x = 0 – 1, QWs and barriers); - $Al_xGa_{1-x}N$ (layers up to 1000 nm, QW barriers and claddings); - Heterostructures: LED, HEMT, diode, photodiode, npn transistors, N-polar devices, waveguide structures; • Restrictions (size, materials prohibited, etc.): - Wafer size: up to 3 × 2″ (batch mode) or 1 × 4″ (single wafer mode);	

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	- Substrate types: sapphire (c-plane, r-plane), patterned sapphire (PSS), SiC (4H/6H), Si (111), graphene-coated templates, bulk GaN/AlN, Si with rare-earth metal oxides; - Prohibited materials: any non-approved precursors or unlisted hydrides; reactor qualified only for III-nitride MOVPE precursors (TMGa, TEGa TMAl, TMIn, NH_3, H_2/N_2). **Cleanroom class:** ISO8 **Contact person:** Dr. Roland Tomašiūnas Institute of Photonics and Nanotechnology Vilnius University roland.tomasiunas@ff.vu.lt	
Atomic layer deposition	**Fiji F200 (Cambridge NanoTech Inc, 2011)**	**FTMC**
	• Substrate size Ø 200 mm, height up to 6.35 mm, multiple substrates that fit the loading bay can be loaded; • Pre-vacuum 10^{-2} mbar; • Operating pressure 1 – 10 mbar (flow through reactor); • Carrier gas: argon (oxygen and nitrogen available for plasma-assisted modes); • 6 Channels for precursors (2 reserved for water and ozone); • Precursor heaters up to 200 °C (metalorganic precursors only); • Deposition temperature 50 – 350 °C; • Available deposition modes: continuous (high speed), exposure (high aspect ratio); plasma-assisted; • Materials allowed: - ALD grade metalorganic precursors in 50 ml Swagelok containers (TMA, TDMAT, TDMAH and similar); - Flat or 3D substrates that fit the loading bay (some substrates may need special holders if uniform deposition is required); - Validated ALD processes: Al_2O_3, TiO_2, HfO_2, Nb_2O_5, - Other materials may be approved after successful process qualification; • Restrictions: Substrates that cause outgassing, corrosive vapours or degrade at the temperatures and pressures achieved during the process. **Contact person:** Laurynas Staišiūnas Department of Electrochemical Materials Science	

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	Center for Physical Sciences and Technology laurynas.staisiunas@ftmc.lt	
Atomic layer deposition	**SAVANNAH 200 (Veeco Instruments Inc.)**	**FTMC**
	• Single-layer and multilayer coatings; • Metal oxide coatings such as SiO_2, HfO_2, TiO_2, etc.; • Physical thickness of coatings from a few nm to a few μm. **Contact person:** Dr. Lina Grinevičiūtė Department of Laser Technologies Center for Physical Sciences and Technology lina.grineviciute@ftmc.lt	
Plasma-enhanced chemical vapour deposition	**PlasmaPro 80 (Oxford Instruments Plasma Technology Ltd., 2019)**	**FTMC**
	• Processes: SiN_x and SiO_2 layer deposition (there is a possibility to deposit amorphous Si); • Growth temperature: 225 – 300 °C; • Chamber temperature: 20 – 350 °C; • Working pressure: 500 – 1500 mTorr; • Maximum substrate size: up to 4”; • Substrates: Silicon, A3B5 (materials with low vapour pressure/ compatible with vacuum chamber); • Deposited layer thickness: 50 – 1500 nm; • Process gases: SiH_4; N_2; Ar; NH_3; N_2O; CF_4; • Plasma generators: High frequency and Low frequency **Cleanroom class:** ISO5 **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	

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Dry Etching

Dry etching is a plasma-based process that removes material from a substrate with high precision and selectivity, unlike wet chemical etching, which uses liquid chemicals and often results in isotropic profiles. Dry etching employs reactive gases (e.g., fluorine, chlorine, or oxygen species) activated by RF plasma to achieve anisotropic profiles, making it ideal for micro- and nano-patterning. Advanced systems allow control over ion energy and gas composition, enabling etching of complex materials such as silicon, oxides, and A3B5 semiconductors while minimising undercutting. Typical applications include semiconductor device fabrication, photonic structures, and nanostructured surfaces.

Inductively Coupled Plasma-Reactive Ion Etching	Plasmalab System100 – ICP 65 (Oxford Instruments Plasma Technology Ltd., 2011)	VU
	• Plasma source: Inductively Coupled Plasma (ICP 65 mm diameter coil, RF 13.56 MHz, up to 1 kW); • Substrate bias: RF 13.56 MHz DC bias supply, up to 600 W (independent from ICP power); • Operating pressure range: typically 1 – 100 mTorr (process dependent); • Gas flow control: 8-line gas pod with individual MFCs, 0 – 200 sccm per channel (process gases: Cl_2, BCl_3, SF_6, O_2, Ar); • Electrode configuration: RF-biased lower electrode with He back-side cooling; upper ICP source with quartz window and match unit; • Backside cooling: Helium pressure 10 – 20 Torr regulated, temperature 15 – 25 °C (via chiller / lower electrode loop); • Process temperature control: chilled electrode (±1 °C stability, water loop); • Vacuum system: turbomolecular pump (typically 700 $L \cdot s^{-1}$) + backing rotary pump (~300 $m^3 \cdot h^{-1}$); base pressure <1 · 10^{-5} mbar; • Process pressure measurement: capacitance manometer (Baratron type) with APC valve feedback; • Endpoint detection: optical (OIPT Verity endpoint system, integrated via PLC I/O per SDM Drawings SE-1040 – 1042); • System control: PC2003 / Blue PLC control software with full interlock monitoring and recipe automation; • Materials allowed:	

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	- III–V compound semiconductors: GaN, AlN, InN, AlGaN, InGaN, InAlN (etching and surface patterning of epitaxial structures grown by MOCVD or MBE); - Group IV materials: Si, SiO_2, Si_3N_4 (etch and cleaning processes); - Metals (selective etch processes): Ti, Al, Ni, Cr, and other thin conductive films (typically in chlorine or BCl_3-based chemistries); - Dielectrics: SiO_2, SiN_x, Al_2O_3 (using fluorine-based plasma chemistries); - Other III–V or dielectric films qualified for dry etch under vacuum; - Wafer size: up to 200 mm (8″) wafers (configured for 2″ – 4″ range at Vilnius University; • Restricted materials: - Any unapproved, corrosive, or pyrophoric gas not included in the qualified process list; - No polymerised organic residues, photoresist-contaminated substrates, or liquids inside the chamber; - No materials that can outgas or contaminate the ICP source (e.g., graphite adhesives, tape residues, or non-vacuum-compatible materials); **Cleanroom class:** ISO8 **Contact person:** Dr. Roland Tomašiūnas Institute of Photonics and Nanotechnology Vilnius University roland.tomasiunas@ff.vu.lt	
Inductively Coupled Plasma-Reactive Ion Etching	**PlasmaPro 100 Cobra** **(Oxford Instruments Plasma Technology Ltd., 2015)**	**FTMC**
	• Processes: - A3B5 semiconductor dry etching; - BCl_3; Cl_2; CH_4 etching processes; • Table temperature: 0 – 60 °C; • Backside cooling: Helium pressure 5 – 15 Torr; • Working pressure: 2 – 50 mTorr; • Process gases: - O_2; N_2; Ar; SF_6; CH_4; H_2; Cl_2; BCl_3; • Plasma generators: - Inductively coupled plasma (ICP) 3000 W; - High frequency plasma (RIE) 300 W; • Sample loading through loadlock; • Maximum sample size: up to 4”;	

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	• Samples: Silicon, A3B5 (materials with low vapour pressure/compatible with vacuum chamber); • Additional information: - Laser endpointing (Horiba LEM G50); - Optical emission spectrum measurement (Ocean Optics USB400). **Cleanroom class:** ISO7 **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	
Reactive Ion Etching	**PlasmaPro 80 (Oxford Instruments Plasma Technology Ltd., 2019)**	**FTMC**
	• Processes: Si_3N_4 and SiO_2 dry etching; • Maximum etching time before cleaning 1 hour; • Working pressure: 20 – 100 mTorr; • Table temperature: 20 °C; - Process gases: O_2; Ar; CHF_3; CF_4; • High frequency plasma generator up to 300 W; • Maximum substrate size: up to 4”; • Samples: Silicon, A3B5 (materials with low vapour pressure/compatible with vacuum chamber). **Cleanroom class:** ISO7 **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	
Plasma Etching and Cleaning System	**PE2000 (South Bay Technology inc., 2016)**	**VGTU**
	• Process: SiO_2 etching (100 – 200 nm/min); • Chamber size: 200 × 100 mm (OD × H); • RF power: 0 – 150 W, manual tuning 13.56 MHz; • Water-cooled electrode; • Vacuum range: $1 \cdot 10^{-3}$ – 1 Torr; • Vacuum system: 2-stage corrosive series, 4.3 litres/min.; • Gas delivery: two channels, stainless steel construction; • Gas control: dual independent control needle valves with safety interlocked solenoid valves;	

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	• Process gases: O_2, CF_4. **Cleanroom class:** ISO5 **Contact person:** Dr. Vaidotas Barzdėnas Faculty of Electronics VILNIUS TECH vaidotas.barzdenas@vilniustech.lt

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Thermal Annealing

Annealing in semiconductor manufacturing is a critical thermal process used to repair crystal damage and activate dopants, ensuring reliable device performance. It involves heating wafers to high temperatures and then cooling them under controlled conditions, thereby correcting lattice defects created during ion implantation and making dopants electrically active. One widely used method is Rapid Thermal Annealing (RTA), in which wafers are heated to temperatures above 1000 °C and then cooled rapidly. This approach minimises unwanted dopant diffusion, enabling the formation of shallow junctions, which are essential for modern, miniaturised transistors. Compared to traditional furnace annealing, RTA provides precise temperature control, shorter cycle times, and improved uniformity. Beyond dopant activation, annealing reduces dislocations and vacancies in the crystal structure, enhancing both electrical and mechanical properties. As devices continue to shrink, advanced annealing techniques like RTA remain indispensable for achieving efficient, stable, and high-performance integrated circuits.

Rapid thermal annealing	UniTemp RTP-100 1200 (UniTemp GmbH, 2011)	VU
	Rapid Thermal Process Oven: • Temperature range: room T – 1200 °C (max temperature 1200 °C); • Ramp-up rate: ≤150 $K \cdot s^{-1}$; • Ramp-down rate: 200 $K \cdot min^{-1}$ (1200 → 400 °C), 30 $K \cdot min^{-1}$ (400 → 100 °C); • Temperature uniformity: ±1.5 % of set temperature; • Heating: top and bottom IR lamps (18 × 1.1 kW, ≈ 20 kW total); • Controller: Siemens SIMATIC® 7″ touch panel, 50 programs × 50 steps each; • Process gases: N_2 (default 5 nlm MFC), optional O_2, Forming Gas (N_2/H_2); • Vacuum capability: ≤10^{-3} hPa; • Cooling: water-cooled chamber + N_2 gas cooling; • Chamber material/size: quartz glass muffle 134 × 169 × 18 mm; • Sample size: single wafer up to 100 mm (4″ diameter); • Materials allowed: - Thermal activation of implanted Si and GaN dopants; - Metal contact alloying (SiAu, SiAl, SiMo); - Rapid thermal oxidation (RTO) / nitridation (RTN); - Crystallisation and densification of thin films; • Annealing of compound semiconductor epilayers; • Restrictions:	

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	- Maximum sample diameter 100 mm (4″); - Chamber height 18 mm – thicker substrates not accepted; - Quartz and metal holders must be clean (ISO 8 protocol; handle with gloves and tweezers); - No unapproved materials or coatings permitted inside the chamber; • Safety: trained technician required. **Cleanroom class:** ISO8 **Contact person:** Dr. Roland Tomašiūnas Institute of Photonics and Nanotechnology Vilnius University roland.tomasiunas@ff.vu.lt	
Rapid thermal annealing	**UniTemp-RTP-1300 (UniTemp GmbH, 2004)**	**FTMC**
	Rapid Thermal Process Oven: • IR lamps (total power 18 kW) are used for heating; • Control with a PID temperature process controller; • Maximum number of steps in a single annealing program: 100; • Temperature modes: - Unlimited time: from room temperature to 700 °C; - Maximum temperature: up to 1100 °C (no longer than one minute!); - Temperature rise rate: programmable, maximum 200 °C/s; - Temperature reduction rate: up to 200 K/s. in the range from 600 °C to 400 °C; - Up to 30 K/s in the range from 400 °C to 100 °C; • Annealing environment: - Heating environment (programmable): vacuum; - Gases: Ultra-pure N_2, Ar (two gas lines, one up to 150 l/min, the other up to 500 l/min); • Materials allowed: Most of the group III-V materials, however, please check with the person in charge before use; • Restrictions: - Heating of samples containing zinc (Zn) is strictly prohibited; - Maximum sample size: 4” diameter wafer with thickness up to 1 mm; - Maximum temperature: up to 1100 °C (no longer than one minute!).	

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	Cleanroom class: ISO7 **Contact person:** Dr. Vaidas Pačebutas Department of Optoelectronics Center for Physical Sciences and Technology vaidas.pacebutas@ftmc.lt	
Rapid thermal annealing	**UniTemp RTP-100-HV (UniTemp GmbH, 2014)**	**FTMC**
	High vacuum compliant Rapid Thermal Process Oven: • Chamber temperature: 20 – 1200 °C ; • Ramp up rate: up to 150 K/s (possible to set up ramp up rate); • Ramp down rate: 1000 °C <T> 400 °C – 2000 °C/min; 400 °C <T> 100 °C – 30 °C/min; • Chamber pressure: atmospheric pressure – up to 10^{-3} mbar; • Chamber size: 100 × 100 × 10 mm (W × H × D); • Materials allowed: - Materials with low vapour pressure/ compatible with vacuum chamber; - Process gases: Ar, N_2; • Restrictions: Maximum sample size: up to 4”. **Cleanroom class:** ISO7 **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	

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Laser-Induced Selective Surface Activation

The Selective Surface Activation Induced by Laser (SSAIL) is a new technology for writing electronic circuits directly on dielectric materials by modifying their surface properties with a laser, developed at the Center for Physical Sciences and Technology. Lasers can write the circuits directly by modifying the surface of polymers, followed by electroless metal plating. SSAIL is a three-step process: the first is surface modification by laser; the second is chemical activation of the laser-modified areas; and the last step is metal deposition by electroless plating.

3D laser processing system with Automatic electroless plating line	AKO3D-1 Compacta 500 (2015)	FTMC
	3D laser microprocessing equipment: • Picosecond solid state Nd: YVO4 laser Femtolux (Ekspla), with II and III harmonics modules. 5 mechanical axis, Polaris controllers, linear STAND axis range 600 mm; • 6-axis robot arm YASKAWA Epx1250 with controller nx100; • Maximum load 5 kg; • Dual-wavelength (1064 nm and 532 nm); • Scanner – intelliSCAN 14 with RTC 5 controller, mounted on a robot arm; Compacta 500 automatic electroless plating line: • 15 tanks 50-liter capacity; • Automatic temperature keeping, filtration, rinsing, heaters; • Copper electroless plating; • Nickel electroless plating; • Immersion Gold deposition; • Ultrasonic rinsing; • Trace width 0.6 – 100 µm; • Many types of polymers, glass, and silicon; • Max size 600 mm; • Circuit writing speed 1000 – 7000 mm/s. **Contact person:** Dr. Karolis Ratautas Department of Laser Technologies Center for Physical Sciences and Technology karolis.ratautas@ftmc.lt	

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Oxygen Plasma Cleaning

Oxygen plasma cleaning is a surface treatment technique that uses low-pressure plasma generated from oxygen gas to remove organic contaminants and improve surface wettability. The process relies on reactive oxygen species and ion bombardment to break down hydrocarbons and other residues without damaging the underlying substrate. It is widely used to prepare samples before thin-film deposition, lithography, or bonding, ensuring high adhesion and cleanliness. Advanced systems enable precise control of plasma power, pressure, and exposure time, making them compatible with sensitive materials and complex geometries. Applications include semiconductor fabrication, microfluidic device preparation, and cleaning of optical components.

Plasma cleaner	**Pico (Diener electronic Plasma-Surface-technology, 2019)**	**FTMC**
	• Chamber size: 120 × 75 × 290 mm (W × H × D); • Samples: Silicon, A3B5 (materials with low vapour pressure/ compatible with vacuum chamber); • Working pressure: 0.2 – 1 mbar; • Process gases: O_2; • Plasma generator: 300 W; • Two operation modes: set up pressure or set up gas flow; • Ability to make and save recipes for different cleaning procedures. **Cleanroom class:** ISO7 **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	
Plasma cleaner	**PDC-002 (Harrick Plasma, 2019)**	**FTMC**
	• Chamber size: 150 × 100 × 165 mm (W × H × D); • Samples: Silicon, A3B5 (materials with low vapour pressure/ compatible with vacuum chamber); • Working pressure: 500 mTorr; • Process gases: O_2, N_2; • Adjustable RF power setting (Low, Medium, High); • Maximum RF power: 30 W. **Cleanroom class:** ISO5 **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies	

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Plasma cleaner	**Tergeo-Plus Tabletop Plasma System (PIE Scientific LLC, 2020)**	**KTU**
	• 75 – 150 W (1 W interval) 13.56 MHz RF power supply with automatic impedance matching (continuous or 100 % to <1 % pulsed plasma modes); • Chamber size: Cylindrical quartz chamber, inner diameter 160 mm, depth 280 mm; • Oxygen service oil pump ultimate pressure <10 mTorr; • MFC gas inlet 0~100 sccm; • Samples: Photoresists, IC/MEMS, 2-D materials, PDMS, Glass, Plastics, bio-polymers, wafers; • Maximum sample size: less than 160 × 280 mm (4” wafer boat and one 6” wafer); • Direct/immersion and remote/downstream mode; • Easy-to-use user interface, ability to make a lot of recipes for different cleaning procedures, and a convenient LCD screen for user input. **Cleanroom class:** ISO5 **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	

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Wafer Level Reliability Testing

Wafer-level reliability testing is a key methodology for assessing the long-term stability and failure mechanisms of semiconductor devices directly on the wafer, before packaging. Precision probe stations in combination with advanced electrical characterisation instruments support a broad range of reliability evaluations.

Probe system with Parameter analyser	**SUMMIT 11000B-AP (Cascade Microtech, 2014) Keithley 4200-SCS Parameter Analyser (Tektronix Inc., 2014)**	**FTMC**
	A semiconductor parameter analyser enables accurate electrical characterisation and reliability testing of device structures. A precise manual probe station enables testing at multiple temperatures. • 4 probes for measurements; • Micromanipulator travel range (X/Y/Z): 12.5 mm / 12.5 mm / 12.5 mm; • Micromanipulator feature resolution <1 µm; • Probe diameter 5 µm; • Table temperature range: from 20 – 350°C; • Optical microscope with magnification up to x400; • Possibility to measure samples in the dark or under irradiation at 400 nm, 460 nm, 523 nm, 621 nm, or 735 nm; • A chamber for measuring samples in dry air or in a nitrogen atmosphere; • Sample size: up to 200 mm width and up to 10 mm height; • DC measurements from 1 pA to 1 A, voltage resolution 1 µV; • Maximum voltage: 200 V; • Pulsed I-V measurements: down to 10 ns; • Capacitance – voltage (C-V) measurements: from 1 pF (10 MHz) to 1 µF (1 kHz). **Contact person:** Dr. Virginijus Bukauskas Department of Physical Sciences Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	
Probe system with Parameter analyser	**Cascade MPS150 (FormFactor / Cascade Microtech, 2025) Keithley 4200A-SCS (Keithley Instruments / Tektronix, 2023)**	**VU**

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	A precise manual probe station with a semiconductor parameter analyser enables accurate electrical characterisation and reliability testing of device structures. • Chuck XY travel: 155 × 155 mm; • XY resolution: 5 µm; • Chuck planarity: <10 µm over 150 mm; • Z-height adjustment (chuck): 10 mm; • Contact/separation stroke: 0 – 3 mm, adjustable; • Rotation: coarse 360°, fine: ±8°, resolution $7.5 \cdot 10^{-3}$ rad; • Microscope travel (manual stage): 50 × 50 mm or 150 × 100 mm, resolution ≤5 µm; platen Z-height adjustment: up to 40 mm; platen separation lift: 200 µm, repeatability <1 µm; • Chuck (Non-thermal, stainless steel): diameter: 150 mm; supported sample sizes: Shards / 1″ to 6″ wafers; surface planarity: ≤ ±3 µm; • Triaxial chuck isolation: >2 GΩ (COAX), >1 TΩ (TRIAX); • Triax residual capacitance: - <20 pF at 3 pA range; - <400 pF at 300 pA range; • Triax leakage: <50 fA (purged enclosure, low humidity); • Triaxial probe arm resistance: >20 TΩ (F-G); • Triaxial probe arm leakage: <5 fA (1σ); • Triaxial capacitance: <1 pF (residual); • Operation voltage: Limited by EC 61010 safety requirements (higher-voltage certificates available on request); • Installed modules (lab configuration): 3 × 4201-SMU (standard low-current SMUs); 1 × 4201-SMU + 4200-PA remote preamplifier; 1 × 4215-CVU (C-V unit, 1 kHz – 10 MHz); 1 × GNDU ground unit; • Voltage / current capability: voltage: ±210 V; current: ±105 mA; • Power: 2.2 W; • Measurement resolution: without preamp: 100 fA; with 4200-PA preamp: 10 aA resolution; • Lowest current ranges (with preamp): 10 nA, 1 nA, 100 pA, 10 pA, 1 pA source-measure ranges; • 4215-CVU (Capacitance-Voltage Unit): frequency range: 1 kHz – 10 MHz; discrete frequencies: 10000, 1 kHz resolution; AC drive voltage: 10 mV – 1 V rms; built-in DC bias: ±30 V (60 V differential); measurement resolution: 1 aF, 1 nS, 0.001° phase; • Optical microscope with magnification up to x50;

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	• Wafers and substrates from 25 mm (1″) to 150 mm (6″). **Contact person:** Dr. Roland Tomašiūnas Institute of Photonics and Nanotechnology Vilnius University roland.tomasiunas@ff.vu.lt	
Probe system	**MicroXact SPS2600 (MicroXact, Inc., 2018)**	**VGTU**
	Semi-automatic wafer probe station for RF and DC characterisation. • Wafer size up to 200 mm; • Temperature range: -60 °C to +300 °C; • Micromanipulator resolution: 0.1 µm; • Optical microscope with digital camera; • RF and DC probing capability; • Vacuum chuck with XYZ control; • Motorised stage with joystick control. **Contact person:** Dr. Vaidotas Barzdėnas Faculty of Electronics Vilnius TECH vaidotas.barzdenas@vilniustech.lt	
Microwave Probe Set	**GGB Industries 40A-GSG (GGB Industries, Inc., 2022)**	**VGTU**
	Integrated with MicroXact SPS2600 and Keysight/Siglent VNA setups for GaN, CMOS, and RFIC testing. • Frequency range: DC – 40 GHz; • Pitch sizes available: 100 µm, 150 µm, 200 µm, 250 µm, 350 µm, 400 µm, 500 µm; • Configuration: there are models for single-ended and differential-ended measurements; • Connector type: 2.92 mm (K) precision coaxial connector; • Contact tip material: BeCu with nickel/gold plating; • Typical insertion loss: <1 dB up to 40 GHz; • Return loss: >15 dB across 0 – 40 GHz band. **Contact person:** Dr. Vaidotas Barzdėnas Faculty of Electronics Vilnius TECH vaidotas.barzdenas@vilniustech.lt	

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Vector network analyser	Siglent SNA5032A (Siglent Technologies, 2023)	VGTU
	A vector network analyser with MicroXact SPS2600 probe station and GGB Industries 40A-GSG microwave probe set enables accurate on-wafer RF and microwave characterisation of high-frequency semiconductor devices and test structures. • Frequency range: 100 kHz – 26.5 GHz; • Dynamic range: >125 dB; • Output power: -55 dBm to +10 dBm; • Measurement parameters: S11, S12, S21, S22; • Display formats: Smith chart, TDR, polar, SWR, log magnitude, phase; • Number of test ports: 2; • IF bandwidth: 1 Hz – 300 kHz, sweep points up to 10,001. **Contact person:** Dr. Vaidotas Barzdėnas Faculty of Electronics Vilnius TECH vaidotas.barzdenas@vilniustech.lt	
Probe system with parameter analyser	**Cascade MPS150-B1A (FormFactor, 2023) FSW85 (Rohde & Schwarz, 2023)**	**KTU**
	Precise manual probe station for RF, mm-Wave and sub-THz characterisation, FA, DWC, MEMS, optoelectronic tests and WLR paired with FSW85 signal and spectrum analyser. • Travel stage 155 × 155 mm (5 µm resolution); • Z height adjustment range 10 mm (0 – 3 mm Z contact separation); • Manual and Programmable Microscope stage (50 × 50 mm, 0.25 µm resolution); • Triaxial probe arms (<50 % humidity, <200 fA leakage current, >1 TΩ resistance (F-G, G-S, F-S), Residual capacitance at 3 pA Tx <20 pF, Capacitance at 300 pA (F-G, G-S) <400 pF). • DCQ probes: power bypass inductance of 8 nH, 3 DC probes, capacitance 100pF; • Infinity probes: DC to 67GHz, maximum DC of 500 mA, thermal range of -65 to 125 ºC; • Parameter analyser frequency range for RF1 input: DC coupled 2 Hz–85 GHz, AC coupled 10 MHz-85 GHz; • Parameter analyser frequency range for RF2 input: DC coupled 2 Hz-67 GHz, AC coupled 10 MHz-67 GHz;	

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	• Parameter analyser frequency resolution of 0.01 Hz. **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Noise source	**NC346E (Noisecom, 2023)**	**KTU**
	Broadband noise source with high temperature and voltage stability designed for noise figure measurement applications. • Frequency: 0.01 - 26.5 GHz; • Output ENR: 19 – 25 dB; • Temperature coefficient: Less than 0.009 dB/°C; • VSWR: Less than 1.50:1; • Voltage coefficient: < 0.002 dB/%ΔV; • I (max): 30 mA **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	

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Packaging

Packaging tools form a critical part of the semiconductor back-end process, where individual chips are assembled, interconnected, protected, and prepared for integration into electronic systems. The packaging tools available in partner institutions support the essential processes that transform a bare semiconductor die into a fully assembled, electrically connected, and mechanically stable device. Together, these tools enable precise die placement, chip interconnection, wafer or die separation, and PCB-level assembly, covering the critical backend steps that follow wafer fabrication.

Scriber	**Micro Diamond Scriber MR-200 (OEG Gesellschaft für Optik, Elektronik & Gerätetechnik mbH, 2015)**	**FTMC**
	Precision micro diamond scriber for exact manual scribing and die separation: • Wafer chuck diameter 100 mm; • Fine adjustment x: ±12.5 mm; y: ±6.5 mm; φ: ±2°; • Fine adjustment XY accuracy 0.01 mm; • Scribing power 10 g – 130 g; • Microscope magnification x8, x40; • Zoom factor: x5; • Resolution of optics better than 10 µm at magnification x40. **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	
Die bonder	**Fineplacer PICO (Finetech GmbH & Co. KG, 2011)**	**FTMC**
	Fineplacer PICO is a multi-purpose, manual die bonder with placement accuracy down to 5 µm: • Manual alignment; • Placement accuracy 5 µm; • Manual placement arm with vacuum; • Available pick-up tools: - Pick-up tool for chip 0.4 × 3 mm; - Pick-up tool for chip 0.4 × 2 mm; - Placement head for laser bars for chip 0.4 × 5 × 0.2 mm; • Placement arm force range 0.1 – 20 N; • Plate with vacuum chuck and heating; • Heating plate temperature up to 420 °C; • Temperature ramp up to 20 K/s; • Nitrogen gas cooling;	

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	• TO56-adapter for heating plate; • Target + chip max thickness 15 mm; • Target size up to 40 × 40 mm. **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt	
Die bonder	**Fineplacer Sigma (TPT Wire Bonder GmbH & Co. KG, 2023)**	**KTU**
	Advanced sub-micron bonder for all types of precision die bonding and flip chip applications at the chip and wafer level: • Accuracy – placement 0.5 µm, alignment 0.1 µm; • Optics – Field of view minimum 3.8 × 2.7 mm, optical resolution 1 µm/px; • Working stage: - X-travel 350 mm; - Y-travel 150 mm; - Z-travel 10 mm; • Bonding force: 0.2 – 40 N; • Heating: chip heating 40 – 450 °C, substrate heating 40 – 500 °C; • UV station – irradiance 300 – 2500 mW/cm^2, angle of irradiation 45° – 130°, angle of illumination 0° – 60°. **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Ultrasonic wire bonding	**Wire bonder HB10 (TPT Wire Bonder GmbH & Co. KG, 2015)**	**FTMC**
	Compact semi-automatic thermosonic wire bonder, with a motorised Z-axis, that supports ball, wedge, bump and ribbon bonding: • Ultrasonic frequency 63.3 kHz; • Ultrasonic power 10 W; • Max. bond force 150 cN; • Bond time 0 – 10 s; • Clamp wire termination; • Wedge-, ball- and ribbon bonding; • Gold-, aluminium wires (silver-, copper wires upon request): - Gold wire ø 50 µm, ø 25 µm; - Aluminium wire 25 µm;	

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	- Gold ribbon 20 × 100 µm; • Automatic bond height adjustment; • Motorised wire spool; • Electronic wire clamp; • Live picture on screen; • Heater stages: ø 60 mm, 100 × 100 mm; • Temperature max: 250 °C. **Contact person:** Dr. Virginijus Bukauskas Department of Physical Technologies Center for Physical Sciences and Technology virginijus.bukauskas@ftmc.lt
Ultrasonic wire bonding	**Wire bonder HB05 (TPT Wire Bonder GmbH & Co. KG, 2021)** — **KTU**
	Benchtop size wire bonder, ideal for laboratories and pilot production lines: • Ultrasonic system – 63.3 kHz transducer PLL control; • Power 0 – 10 W; • Bonding time 0 – 20000 ms; • Bonding force 5 – 200 g; • Wires – gold and aluminium wires (17 – 75 µm); • Gold ribbon (up to 20 × 200 µm); • Motorised wire spool (50.8 mm); • Wire termination via clamp tear; • Wire feed angle 90°; • Throat depth 165 mm; • Travel stage – fine table motion 15 mm; • Temperature controller up to 250 °C (±1 °C); • Max component width – 400 mm. **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt
Ultrasonic wire bonding	**Wire bonder HB100 (TPT Wire Bonder GmbH & Co. KG, 2022)** — **KTU**
	Automatic wire bonder with motorised Z-Y-X Axes and bond head rotation: • Ultrasonic system – 63.3 kHz transducer PLL control; • Power 0 – 10 W; • Bonding time 0 – 5000 ms; • Bonding force 10 – 200 g; • Wires – gold and aluminium wires (17 – 75 µm);

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	• Gold ribbon (up to 25 × 250 µm); • Motorised wire spool (50.8 mm); • Wire termination via bond head tear or clamp tear; • Wire feed angle 90° with 14 mm immersion depth; • Travel stage – Z-Drive travel of 100 mm (0.5 µm resolution) and X-Y Drive travel of 100 mm (0.1 µm resolution); • Rotation-Drive resolution ±0.5°; • Temperature controller up to 200 °C (±1 °C); • Max component width – 400 mm. **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Micro Placer	**MPL3100 (Essemtec AG, 2016)**	**VGTU**
	Semiautomatic microplacer for BGA, CSP and fine pitch components: • Placement accuracy: ±5 µm; • Component range: 0201 to 45 × 45 mm, bare dies, flip chips, µBGAs; • PCB size: up to 400 × 300 mm; • Placement speed: up to 3000 components/hour (semi-automatic); • Integrated vision system for component and pad alignment; • Adjustable vacuum pickup with programmable Z-axis control; • Support for adhesives and solder paste dispensing (optional). **Contact person:** Dr. Vaidotas Barzdėnas Faculty of Electronics Vilnius TECH vaidotas.barzdenas@vilniustech.lt	
Materials Printer	**DMP-2850 (Fujifilm Dimatrix, 2022)**	**KTU**
	Dimatix materials printer designed for precise functional fluid deposition on various ceramics, glass, plastic and flexible materials: • Printable area: 210 mm x 315 mm, when substrate thickness < 0.5 mm and 210 mm x 260 mm, when substrate thickness is 0.5-25 mm;	

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	• Repeatability: ± 25 µm; • Substrate holder temperature: ambient to 60°C; • System Footprint: 673 mm x 584 mm x 419 mm; • Fiducial Camera; • Piezo-driven jetting device with integrated reservoir and heater; • Usable ink capacity: up to 1.5 ml; • Materials compatibility: many water-based, solvent, acidic or basic fluids; • Cartridge nozzles: 12, single row, 75 DPI, 2.4 pL drop volume, 30 µm dot size. **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Stencil printer	**IWT Accella (Speedline, 2013)**	**KTU**
	Stencil printer designed for surface mount technology (SMT) systems for large-scale PCB assembly: • Maximum substrate weight: 7kg; • 3-stage transport rail system; • Total system alignment: ±12.5 µm; • Wet print deposit: ±25 µm; • Cycle time: less than 5.5 s; • Maximum board size: 558 x 508 mm; • Minimum board size: 50.8 x 50.8 mm; • Board edge clearance: configurable to 3 mm or 5 mm; • Transport height from floor: 813 mm to 1041 mm; • Snap-off: -0.025 mm to 12.7 mm • Print Speed: 6 mm/s to 305 mm/s; • Print Stroke: ±280 mm; **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Pick & Place	**NXT-1 (Fuji, 2005)**	**KTU**
	Pick & place machine designed for surface mount technology (SMT) systems for large-scale PCB assembly: • PCB Size: From 48mm x 48mm to 510 mm x 534mm;	

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	• Patch speed: H12HS - 22500, H08 - 10500, H04 - 6500; H01 - 4200; • Patch accuracy: H12S / H08 / H04: 0.05mm (3 sigma) cpk ≥ 1.00; • Patch range: H12S - ~7.5x7.5mm high; H08 - ~12x12mm high, H04 - ~38x38mm high, H01/H02/OF - ~74x74mm, G04 - ~15.0mmx15.0mm high; • Mounted rack: maximum of 20 species/module (8mm tape conversion); • Air flow rate: 0.5 MPa; • LED mounter. **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Reflow oven	**V8 Nitro 3.2 B (Rehm, 2004)**	**KTU**
	Reflow oven designed for surface mount technology (SMT) systems for large-scale PCB assembly: • Heating zone length 3200 mm; • Maximum permissible soldering temp.: 300°C for preheating zones and 350°C for peak zones; • Cooling zone length 1000 mm (two-stage, water-cooled); • Conveyor system width (single): min. 50 mm to max. 400 mm; • Conveyor speed: 180-1800 mm/min.; • Width of a mesh belt conveyor: 400 mm; • Clearance above the mesh belt conveyor: 30 mm; • Interface: Siemens. **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	
Pick & Place	**Expert M (Essemtec AG, 2016)**	**VGTU**
	Manual and semiautomatic SMD assembly system for prototyping: • Placement accuracy: ±0.05 mm; • Component size range: 0201 to 50 × 50 mm; • PCB size: up to 400 × 300 mm; • Placement rate: up to 400 components/hour (operator dependent);	

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	• Integrated vacuum pickup with footswitch control; • Rotational θ adjustment and mechanical alignment system; • Support for tape, stick, and loose components. **Contact person:** Dr. Vaidotas Barzdėnas Faculty of Electronics Vilnius TECH vaidotas.barzdenas@vilniustech.lt	
Solder paste printer	**Uniprint-M (Uniprint, 2016)**	**VGTU**
	Manual solder paste printer. • Printing area: up to 400 × 300 mm; • Printing method: manual squeegee pressure and alignment; • Alignment accuracy: ±0.02 mm (manual micro-adjust); • Frame size compatibility: 370 × 470 mm typical; • Suitable for single and double-sided PCB printing; • Adjustable PCB holder with X/Y and theta control; • Material: anodised aluminium with vacuum or clamp fixation. **Contact person:** Dr. Vaidotas Barzdėnas Faculty of Electronics Vilnius TECH vaidotas.barzdenas@vilniustech.lt	
Reflow oven	**RO06-Plus (Essemtec AG, 2016)**	**VGTU**
	Batch reflow oven for prototyping and low-volume manufacturing: • Maximum temperature: 350 °C; • Heating zones: 6 (4 top, 2 bottom); • Temperature accuracy: ±1 °C; • PCB size: up to 320 × 220 mm; • Reflow profiles: leaded and lead-free solder compatible; • Cooling system: integrated forced-air cooling; • Control: digital process controller with LCD display. **Contact person:** Dr. Vaidotas Barzdėnas Faculty of Electronics Vilnius TECH vaidotas.barzdenas@vilniustech.lt	

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3D ceramic printer with muffle furnaces	**C101 Hybrid (3DCERAM SINTO, 2023) HCV56/12 (Hobersal, 2023) XG3/8 (Hobersal, 2023)**	**KTU**
	3D ceramic printer with muffle furnaces designed for various packaging enclosure fabrication and sintering, with the ability to print 2 materials simultaneously on the same layer and optimisation of the printing precision elements: • Build platform size 100 x 100 x 150 mm; • UV laser power 300 mW; • UV laser spot size ≈ 60 µm; • UV laser wavelength 405 nm; • Z axis movement 0.020 - 0.125 mm; • Muffle furnace volume 3-56 l; • Heating: 1200-1800 °C (1100-1700 °C continuous); • 3 heating zones. **Contact person:** Šarūnas Jankauskas Proto Lab, M-Lab Kaunas University of Technology sarunas.jankauskas@ktu.lt	

4 CONCLUSIONS

This Database of Resources documents the technological processing equipment and design tools available across the four ChipsC²-LT consortium partners, providing comprehensive capabilities for semiconductor research, development, and prototyping. The inventory demonstrates that the consortium covers the key stages of the semiconductor value chain, from IC design and epitaxial growth through wafer processing and packaging to electrical and RF characterisation.

Key strengths of the combined infrastructure include III-V compound semiconductor epitaxy (MBE and MOCVD), nanometre-resolution lithography, industrial-grade EDA tools with access to foundry PDKs, and wafer-level testing up to 26.5 GHz. Cleanroom facilities, ranging from ISO 5 to ISO 8 classification, support processing requirements across different technology areas. The distributed infrastructure across Vilnius and Kaunas provides both redundancy and depth of specialisation.

This inventory establishes the baseline for ChipsC²-LT's one-stop-shop service model. Subsequent updates will incorporate characterisation and advanced testing equipment to complete coverage of the value chain. The following steps include developing resource management procedures (D2.7, M12), documenting infrastructure upgrades (D2.2, M12),

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and defining the detailed service portfolio in the four focus areas (D2.4, M12). As the Competence Centre establishes connections with European pilot lines and the ENCCC network, access to additional external resources will complement the capabilities documented here.

5 APPENDICES

5.1 Abbreviations

Abbreviation	Full Form
ASIC	Atomic Layer Deposition
CCC	Chips Competence Centre
CVD	Chemical Vapour Deposition
EDA	Electronic Design Automation
ENCCC	European Network of Chips Competence Centres
FTMC	Center for Physical Sciences and Technology
GaN	Gallium Nitride
ICP	Inductively Coupled Plasma
KTU	Kaunas University of Technology
MBE	Molecular Beam Epitaxy
MOCVD	Metal-Organic Chemical Vapour Deposition
PDK	Process Design Kit
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PVD	Physical Vapour Deposition
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
SiC	Silicon Carbide
SME	Small and Medium-sized Enterprise
VNA	Vector Network Analyser
VU	Vilnius University
VGTU	Vilnius Gediminas Technical University

5.2 References

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3. ChipsC²-LT Consortium (2025). D1.1 Management and Quality Plan.
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